**Hardware Development Plan**

1. **Scope:**  
   The following plan lays out the how the team will approach the CAN controller project. The second section defines the purpose of this project. The third section will cover the standards that apply to this project. The fourth section covers how life cycle data will be tracked throughout the development cycle. The fifth and final section covers the different software and tools that will be used throughout the project.
2. **Purpose:**  
   The primary purpose of the project is for all team members to become familiar with CAN protocol. Secondary purposes include gaining further exposure to DO-254 standards, System Verilog, as well as Agile development and Jira.
3. **Standards:**

The following documents will define the standards for this project with regards to coding practices, requirements generation, and branching strategies.

* 1. [Coding Standards](https://lnttsgroup.sharepoint.com/sites/LTTS-Collins-FPGATraining/_layouts/15/Doc.aspx?sourcedoc=%7BD717F7B6-E49C-4A3D-8979-9C33B494EDD0%7D&file=Coding%20Standards.docx&action=default&mobileredirect=true&CT=1591630910639&OR=ItemsView).v2
  2. [Requirements Standards](https://lnttsgroup.sharepoint.com/sites/LTTS-Collins-FPGATraining/_layouts/15/Doc.aspx?sourcedoc=%7B9B8D3923-8CBC-4A8B-835B-5399245B6A96%7D&file=Requirements%20Standards.docx&action=default&mobileredirect=true&CT=1591630925910&OR=ItemsView).v2
  3. [Branching Strategy Standards](https://lnttsgroup.sharepoint.com/sites/LTTS-Collins-FPGATraining/_layouts/15/Doc.aspx?sourcedoc=%7B2C639C94-C1F3-44DD-9050-C09DAD3E4F11%7D&file=Branching%20strategy.docx&action=default&mobileredirect=true&CT=1591630951111&OR=ItemsView).v2

1. **Life-Cycle Data:**

The following is how we will track the progress of our project. As the project evolves we will record life-cycle data to analyze and draw conclusions from upon completion of the project and each sprint.

* 1. Life-Cycle Tracking Metrics:
     1. Number of git commits and new or edited lines of code shall be recorded at the end of each sprint.
     2. A Review Tracking Tool developed in Python shall be used in unison with GitHub to track the review and approval of different task.
     3. Jira *Sprint Reports* and *Velocity Charts* shall be saved at the end of each sprint.
     4. A *Cumulative Flow Diagram* shall be saved at the conclusion of the project.
  2. Project Phases:
     1. Phase 1: Preparation Deadline
        1. Jira & GitHub Setup------------------------------------- 6/29/2020
        2. System Specifications-----------------------------------7/01/2020
        3. Functional Requirements------------------------------7/10/2020
        4. Test Case Generation-----------------------------------7/10/2020
     2. Phase 2: Development
        1. Module Development & Validation----------------7/22/2020
        2. Top Level Integration----------------------------------7/23/2020
        3. Functional Verification--------------------------------7/26/2020
        4. Synthesis & FPGA Implementation----------------7/29/2020
        5. Final-------------------------------------------------------7/31/2020
  3. Development Notes:
     1. Modules have 4 major development milestones each of which must pass a review with checklist before continuing. Milestones & Checklist Templates:
        1. Milestone 1: Requirements, [Requirements Checklist Template](https://lnttsgroup.sharepoint.com/sites/LTTS-Collins-FPGATraining/_layouts/15/Doc.aspx?sourcedoc=%7B02D390B2-6A58-45B4-99A7-8633A58EF847%7D&file=Requirements%20Checklist.docx&action=default&mobileredirect=true&CT=1593551449443&OR=ItemsView)
        2. Milestone 2: Testcases , [Testcases Checklist Template](https://lnttsgroup.sharepoint.com/sites/LTTS-Collins-FPGATraining/_layouts/15/Doc.aspx?sourcedoc=%7B1DC82F3D-DEAC-4AF4-B161-87DC0DE5CC18%7D&file=Testcases%20Checklist.docx&action=default&mobileredirect=true&CT=1593551546838&OR=ItemsView)
        3. Milestone 3: Validation, [Validation Checklist Template](https://lnttsgroup.sharepoint.com/:w:/r/sites/LTTS-Collins-FPGATraining/_layouts/15/Doc.aspx?sourcedoc=%7BEB526083-7186-4D3A-8FEA-892B5B748509%7D&file=Validation%20Checklist.docx&action=default&mobileredirect=true)
        4. Milestone 4: Verification, [Verification Checklist Template](https://lnttsgroup.sharepoint.com/sites/LTTS-Collins-FPGATraining/_layouts/15/Doc.aspx?sourcedoc=%7B6E61FB6A-D82D-4B5D-A85C-EE340C51D6F8%7D&file=Verification%20Checklist.docx&action=default&mobileredirect=true&CT=1593551640849&OR=ItemsView)
     2. A simulation testbench shall be developed during the Module Development & Validation section, this is used to display the modules function within the top level design. This testbench is not included in release versions and is not the subject of any checklist, it is strictly to assist in the review process.
     3. During the review process for requirements, testcases, validation, and verification Checklist shall be attached as conversation comments in GitHub.
     4. Feedback for Requirements and testcase review shall be done as standard review comments within GitHub.
     5. Feedback for Source code shall be done as review comments but attached to specific lines within the source code (In the GitHub Review Tool this is done by clicking the blue ‘+’ next to the line of code then selecting “start a review” or “add review comment”).

1. **Development Environment and Tools:**

Below is a list of the tools the team will use as well as how or when they will be utilized during the project.

* 1. Requirements: Requirements are written in Excel according to the standards above and then signed off on using a checklist in Word.
  2. Design: Design and functionality specifications are written in word.
  3. Coding: Xilinx Vivado shall be used for developing, compiling, and testing our source code.
  4. Compiler/Linker: xsim shall be used when simulating source code.
  5. Code Review: Code Striker will be used to track code review processes for module and test bench development.
  6. Task Management: Use Jira to manage and assign task to team members.
  7. Version Control: Github shall be used for version control and bug tracing
  8. Hardware: Digilent Nexys A7 shall be used for FPGA integration.